REMARKS

Claims remaining in the present patent application are numbered 1-23. The rejections and comments of the Examiner set forth in the Office Action dated May 7, 2004 have been carefully considered by the Applicants. Applicants respectfully request the Examiner to consider and allow the remaining claims.

35 U.S.C. §103 Rejection

The present Office Action rejected Claim 1 under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. (U.S. Patent No. 6,140,992), in view of Kim et al. (U.S. Patent No. 5,355,443), and Singla et al. (U.S. Patent No. 6,597,373). Also, Claims 2-4, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. in view of Kim, Hannah (U.S. Patent No. 5,038,297), and Yuki et al. (U.S. Patent No. 5,805,149), further in view of Ogawa et al. (U.S. Patent No. 6,018,331) and Singla et al. Further, Claims 5, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. in view of Kim et al. and Hannah; Yuki et al. and Singla et al. Moreover, Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. in view of Kim et al. and Hannah, further in view of Ogawa et al., and Singla et al. Also, Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. in view of Kim et al. and Hannah and Yuki et al., further in view of Ogawa, Singla, and He et al. (U.S. Patent No. 6323,849).

Applicants have reviewed the above cited references and respectfully submit that the present invention, as recited in Claims 1-23, is neither anticipated nor rendered obvious by the Matsuzaki et al. reference taken alone or in combination

with the Singla et al., Kim et al., Hannah, Yuki et al., Ogawa et al., and He et al. references.

Independent Claims 1, 10, and 18

Applicants respectfully point out that embodiments of the present invention as claimed in amended independent Claims 1, 10, and 18 each recite, in part:

> A display unit comprising:
> a display panel comprising a pixel matrix comprising: an (m x n) pixel frame buffer region; and an x pixel border region for only displaying a display attribute, wherein said border region surrounds said frame buffer region . . .
> a border attribute register for containing said display attribute for said border region, wherein said display attribute is selected to provide viewing contrast with image data located near said border region . . . (Emphasis Added)

Specifically, the claimed embodiments of the present invention pertain to a controllable pixel border that surrounds a frame buffer region for improved viewability of a display device. That is, the pixel border displays a display attribute. For instance, the pixel border is useful for increasing viewability, e.g., contrast, of images and/or characters that are displayed along the edge of a frame buffer region.

In particular, embodiments of the present invention as claimed in independent Claims 1, 10, and 18, recite, unlike the prior art references which do not disclose a controllable pixel border region, a pixel border region that displays a display attribute that is selected to provide viewing contrast with images and/or characters in the pixel frame buffer region that are located near the pixel border region (See Specification, page 20 lines 1-2).

Applicants respectfully note that the prior art reference, Matsuzaki et al., does not teach nor suggest a controllable pixel border region that provides viewing contrast. The Matsuzaki et al. reference discloses a display control system for controlling the display format to be displayed by a display apparatus. As such, the Matsuzaki et al. reference discloses a border section that displays border pixel data to frame a display image frame. However, Applicants respectfully point out the Matsuzaki et al. reference does not teach or suggest a pixel border region displaying a display attribute that is selected to provide viewing contrast with images and/or characters near the border region, as in embodiments of the present invention as claimed in independent Claims 1, 10, and 18.

The present Office Action rejected independent Claims 1, 10, and 18 primarily because it is argued that the Matsuzaki et al. reference "at least suggests a pixel border region displaying a display attribute (e.g., color that is selected to provide viewing contrast." Specifically, the present Office Action on page 10 argues a pixel border region providing viewing contrast as follows:

> In response to the arguments in (A), Matsuzaki teaches selecting/switching one of the display formats (Matsuzaki column 2); setting the format of the binary border pixel data in color bits different from the effective display region (to provide viewing contrast; see Matsuzaki column 3 and 6) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6, 7).

First, for clarification, Applicants understand that the Matsuzaki et al. reference discloses the selection or switching between display formats, such as "[1024 pixels (lateral direction) x 768 lines (vertical direction)], [800 pixels (lateral direction) x 600 lines (vertical direction)], and the like. (See Matsuzaki et al.

reference col. 2, lines 4-10). That is, the Matsuzaki et al. reference discloses the switching of display formats that define resolution on a display during a display operation, and not color formats as argued in the present rejection.

Second, Applicants respectfully assert that the Matsuzaki et al. reference does not disclose the "setting [of] the format of the binary border pixel data in color bits different from the effective display region [to] provide viewing contrast," as stated on page 10 of the present Office Action. Applicants respectfully request the Examiner to specifically point out where in columns 3 or 6 does the Matsuzaki et al. reference disclose that the color bits in the binary border pixel data are set to be different from the effective display region to provide viewing contrast.

In contrast, Applicants respectfully assert that the format of the binary border pixel data and the effective display data are identical. Specifically, Applicants respectfully assert that the Matsuzaki et al. reference discloses the conversion of display data, using an existing SVGA as an FLCD (ferroelectric liquid crystal display) interface, to pixel data for an FLCD display. That is, the Matsuzaki et al. reference discloses the conversion of multivalue display data of 256 gradations expressed by eight bits for each color (red [R], green [G], and blue [B]) down to binary pixel data corresponding to each pixel in the display image frame of the FLCD. That is, the display data is converted to be compatible with the FLCD display, such that the format of each color of a pixel is converted from 8 bits down to binary pixel data.

Additionally, the Matsuzaki et al. reference discloses that a separate "border producing circuit 25 produces pixel data of a border section in the FLCD display image frame." (See Matsuzaki et al., col. 7, lines 12-13). Necessarily, as stated,

the format of the pixel data of the border section is compatible with the FLCD display image frame. While the specific format of the pixel data of the border section is not disclosed in the Matsuzaki et al. reference, Applicants respectfully assert that the format of the pixel data of the border section should be identical to the format of the display data that is converted from 8 bits down to binary pixel data. In that way, both the display data and the pixel data of the border section can be displayed in the FLCD display image frame. As such, the Matsuzaki et al. reference discloses producing pixel data of a border section of a pixel format that is compatible with the FLCD display image frame, but does not disclose or suggest producing pixel data of a border section of a color format that provides viewing contrast with the display data, as recited in independent Claims 1, 10 and 18 of the present invention.

Moreover, the present Office Action states that the format of the "synthesized pixel data in the border section" is produced as an 8-bit parallel data by the border producing circuit 25, which is in contrast to the pixel display data from the binarizing half tone processing circuit 26. Applicants respectfully assert that the 8-bit parallel data is the format used when transferring both the pixel data of the border region and the effective display region. Applicants respectfully assert that this transfer format is different than the format of the pixel data of both the border region and the effective display region, which is the binary pixel data as previously described. Moreover, upon transfer, both the pixel data of the border region and the effective display region follow the same 8-bit parallel data format. The specific text which describes the 8-bit parallel data is as follows:

> Fig. 9 shows a state in which the display line address and the pixel data are transmitted to the FLCD 20. In the embodiment, it is shown on the assumption that the display line address and the pixel

> data are transmitted as 8-bit parallel data of AD0 to AD7 to the FLCD20. (See Matsuzaki et al., col. 7, lines 39-43).

That is, the Matsuzaki et al. reference discloses that pixel data for both the border region and the effective display region are transmitted as 8 bit packets in parallel over the 8 address lines to the FLCD, as shown in Figure 9. As such, there is no distinction between the pixel data of the border region and the effective display region upon transfer, as is implied by the present Office Action.

In addition, Applicants respectfully assert that the implication in the present Office Action that the "synthesized pixel data in the border section" is somehow different than the pixel data from the binarizing half tone processing circuit is incorrect. The particular statement in the present Office Action is as follows: "and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6, 7)."

In contrast to the present Office Action, Applicants respectfully present the following paragraph that describes the synthesizing process to serialize the pixel data in the border section with the pixel data in the effective display region:

> The border pixel data produced by the border producing circuit 25 is serially synthesized with the pixel data from the binarizing half tone processing circuit 26 by a synthesizing circuit 27. Further, a display line address from the line address producing circuit 24 is synthesized to the resultant synthetic data by a synthesizing circuit 28. After that, the synthesized data is sent to the FLCD 20. (See Matsuzaki et al., col. 7, lines 32-28).

That is, pixel data in the border section is not "synthesized pixel data." However, the pixel data in the border section is synthesized with the pixel data from

binarizing half tone processing circuit (the display data) to produce "synthesized data." As such, the synthesized data includes the pixel data for both the border section and the effective display region.

Moreover, the implication that the synthesizing process in the Matsuzaki et al. reference somehow provides viewing contrast is incorrect. Applicants respectfully point out that the synthesizing process is to serialize the border pixel data and the pixel data from the binarizing half tone processing circuit. That is, as shown in Figure 7B, the data format of a display line which includes both border pixel data and pixel data of the effective display region is serialized, as follows: "in the display line (B), since both edge portions are included in the border section, it has a data format such that after the line address, border pixel data, pixel data, and border pixel data continue in accordance with this order." (See Matsuzaki et al., col. 7, lines 27-31). As such, the serialization process in the Matsuzaki et al. reference does not provide any viewing contrast between the pixel data of the border region and the effective display region, as in independent Claims 1, 10, and 18, but only serializes the pixel data that is then sent to the FLCD.

As such, the Matsuzaki et al. reference does not disclose any difference or distinction in color between pixels in the border region and the effective display region for viewing contrast, as recited in independent Claims 1, 10, and 18 of the present invention. Thus, Applicants respectfully submit that the present invention as disclosed in independent Claim 1 is not rendered obvious by the Matsuzaki et al. reference.

Moreover, the Singla et al. reference fails to remedy the shortcomings of the Matsuzaki et al. reference. Specifically, Applicants respectfully note that the prior

art reference, Singla et al., does not teach nor suggest a controllable pixel border region that provides viewing contrast. In contrast to independent Claims 1, 10, and 18 of embodiments of the present invention, the Singla et al. reference discloses a display controller that is capable of generating image borders based on scanning resolution information. Importantly, the Singla et al. reference determines the appropriate image border based on the resolutions of the image and display device. That is, the resolutions define appropriate x and y coordinates of both the image and the border region and not color, as follows:

> The display TG uses this data to determine the image resolution (X_IMAGExY_IMAGE). The display TG then determines the values shown in FIG. 2 that define border region 106 using the image and display resolutions: X_BORD1, X_BORD2, Y_BORD1, and Y_BORD2. (See col. 3, lines 38-40, and Figure 2 of the Singla et al. reference)

Further resolution for both the pixel border and the displayed image is described in the Singla et al. reference in terms of pixel resolution and not color, as follows:

> As shown in FIG. 1, a display 102 has a resolution of a number of pixels along the x-axis given by X_DISPLAY and along the y-axis given by Y_DISPLAY. For example, an LCD may have a resolution of 1024x768 pixels (i.e., X_DISPLAY =1024, and Y_DISPLAY = 768). Similarly, an image 104 has a resolution of a number of pixels along the x-axis given by X_IMAGE and along the y-axis given by Y_IMAGE. For example, a VGA image may have a resolution of 640x480 pixels (i.e., X_IMAGE=640, Y_IMAG=480). (See col. 2, lines 64 through col. 3, line 6 of the Singla et al. reference)

As such, the Singla et al. reference refers to an x and y border resolution, and resolution attribute, of an image border, and does not teach nor suggest a pixel border region displaying a display attribute that is selected to provide viewing contrast with images and/or characters near the border region, as in embodiments of the present invention as claimed in independent Claims 1, 10, and 18.

Applicants agree that the Singla et al. reference discloses a solid single-color border surrounding the image in column 8. That is, the border consists of a solid single-color that is static and unchangeable from image to image. However, Applicants respectfully assert that the Singla et al. reference does not teach the claim limitation of a pixel border region displaying a display attribute (color) that is selected to provide viewing contrast with images and/or characters near the border region, as stated in the present Office Action. Instead, Applicants assert that the predetermined border scheme, by user override, is adjusted for user preferences. That is, the border scheme can be adjusted for the user to select a static color for the border region, according to the "user preferences." Thus, Applicants respectfully assert that the selectable color as determined by the "user preferences" does not provide viewing contrast between the border and the image data located near the border region, as recited in independent Claims 1, 10, and 18.

Moreover, the Kim et al., Hannah, Yuki et al., Ogawa et al., and He et al. prior art references also do not teach, suggest, or disclose a pixel border region displaying a display attribute that is selected to provide viewing contrast with images and/or characters near the border region, as in embodiments of the present invention as claimed in independent Claims 1, 10, and 18.

Dependent Claims 2-4

As to Claims 2-4, Applicants respectfully assert that the prior art references do not teach, suggest, or disclose a second set of signals being generated within invalid timing windows with respect to the frame buffer region, wherein the second set of signals are for displaying the display attribute for viewing contrast within the border region. In particular, each of the prior art references, Singla et al., Ogawa,

and Yuki et al., disclose the generation of a second set of signals within blanking timing windows, etc. for display within a frame buffer region that is designated as a border to an image. That is, in each of the prior art references, border data is generated for display within the frame buffer region. As such, in each of the prior art references, pixels designated as a border at one time in the frame buffer region, can be designated as a displaying image data at another time in the frame buffer region.

In contrast, embodiments of the present invention in dependent Claims 2-4 disclose the generation of a second set of signals within invalid timing windows of the frame buffer region, wherein the second set of signals are for displaying a display attribute that provides viewing contrast in a border region that is separate from the frame buffer region. That is, the x pixel border region is for displaying border display attributes only and not image data.

Dependent Claims 11 and 12

For analogous arguments set forth in relation to dependent Claims 2-4, Applicants respectfully contend that the prior art references, Singla et al., Ogawa, and Yuki et al., do not teach, suggest, or disclose a second set of signals being generated within invalid horizontal and vertical timing windows of a first set of signals used for rendering character images within a frame buffer region, wherein the second set of signals are for displaying a display attribute that provides viewing contrast in a border region that is separate from the frame buffer region, as is disclosed in embodiments of the present invention of dependent Claims 11 and 12. That is, pixels in the frame buffer region are for displaying images, and pixels in the x-pixel border region are for only displaying border attribute data, and never image data.

Dependent Claims 19 and 20

For analogous arguments set forth in relation to dependent Claims 2-4 and Claims 11 and 12, Applicants respectfully contend that the prior art references, Singla et al., Ogawa, and Yuki et al., do not teach, suggest, or disclose a second set of signals being generated within video timing windows that contain invalid data of a first set of signals used for rendering character images within a frame buffer region, wherein the second set of signals are for displaying a display attribute that provides viewing contrast in a border region that is separate from the frame buffer region, as is disclosed in embodiments of the present invention of dependent Claims 19 and 20. That is, pixels in the frame buffer region are for displaying images, and pixels in the x-pixel border region are for only displaying border attribute data, and never image data.

Thus, Applicants respectfully contend that embodiments of the present invention as claimed in independent Claims 1, 10, and 18 are neither anticipated nor rendered obvious by the Matsuzaki et al., taken alone or in combination with the Singla et al., Kim et al., Hannah, Yuki et al., Ogawa et al., and He et al. references, and are in a condition for allowance. As a result, Applicants respectfully submit that Claims 2-9 which depend from independent Claim 1, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim. Also, Applicants respectfully submit that Claims 11-17 which depend from independent Claim 10, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim. Further, Applicants respectfully submit that Claims 19-23 which depend from independent Claim 18, as currently amended, are also in a condition for allowance as being dependent on an allowable base claim.

CONCLUSION

In light of the facts and arguments presented herein, Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-23 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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